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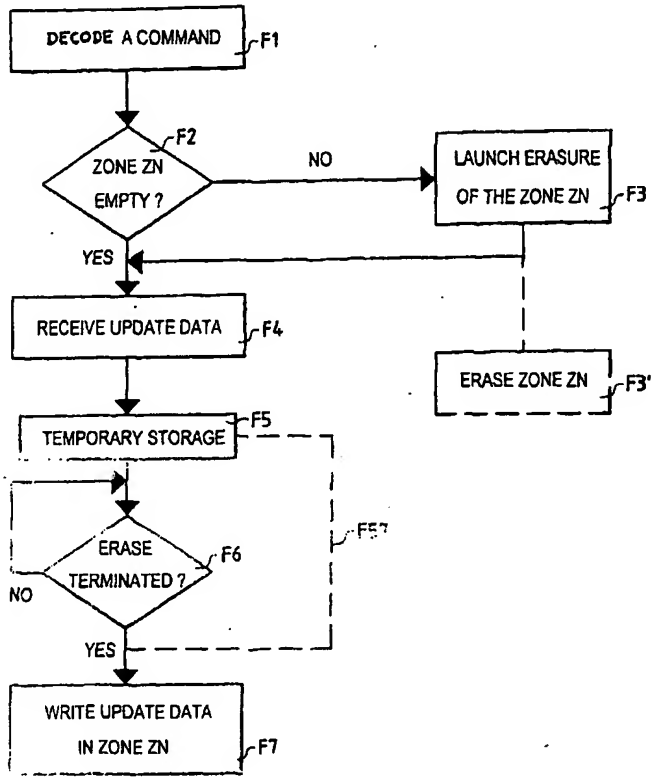
(54) Title: METHOD PF PROCESSING A WRITE COMMAND



(57) Abstract: A write command comprises a definition of a memory zone (ZN) followed by data to be stored in that memory zone. Such a write command may be, for example, a write command in accordance with ISO 7816 standard relating to smart cards. The write command is processed in the following manner. In a receiving step (F4), the data is written into a buffer memory (RAM). In an erasure step (F3), the memory zone (ZN) defined by the write command is erased while the data is written into the buffer memory (RAM). Thus, the receiving step (F4) and the erasure step (F3) are, at least partially, effected in parallel. In a transfer step (F7), the data is transferred from the buffer memory (RAM) to the memory zone (ZN) defined by the write command.

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METHOD PF PROCESSING A WRITE COMMAND

FIELD OF THE INVENTION

The present invention relates to the processing of a write command that comprises a definition of a memory zone followed by data to be stored in that memory zone. Such a write command may be, for example, a write command in accordance with ISO 7816 standard relating to smart cards.

BACKGROUND OF THE INVENTION

Smart cards generally comprise an electrically erasable programmable read-only memory (EEPROM). EEPROMs store data in non-volatile manner such that the data remains recorded in the memory even when the memory is unpowered. They also allow data to be updated by erasing all or part of the memory and by writing new data. The erase operation is performed electrically by applying a high voltage to the memory.

Figure 1 is a block diagram of the electrical portion of a smart card. The circuit shown in Figure 1 comprises a microcontroller 1 constituting the electronic chip of the card, and an interface 2 enabling the card to communicate with a read/write terminal (not shown).

The microcontroller 1 mainly comprises a microprocessor 10, memory units 20, 30, 40, an input/output circuit 50, and a data bus 60 connecting the circuits 20, 30, 40, and 50 to the microprocessor 10. The memory units 20 and 30 respectively comprise a read-only memory (ROM) containing a computer program known as the "operating system" which governs operation of the chip, and a random access memory (RAM) for temporary storage of data being processed by the microprocessor 10.

The EEPROM unit 40 serves to store data specific to the user, such as name, secret code (PIN), or a sum of money that is available. With reference to Figure 2, the memory 40 includes in particular an EEPROM 400, a

voltage-raising module 410 for erasing data stored in the memory 400, and a register 420 containing a flag whose binary "0" or "1" state indicates whether the process of erasing the memory 400 has terminated or not.

The interface 2 can be constituted by electrical contacts suitable for co-operating with corresponding electrical contacts of a read/write terminal, and/or by radio transceiver means suitable for interchanging radio signals with the terminal, where such transceiver means are said to provide "contactless" connection. A smart card equipped for contactless connection can be used, for example, as an electronic purse. The user can then perform a transaction such as purchasing an article, by passing the card into an electromagnetic field produced by the terminal and serving, amongst other things, to power the chip with electricity.

Figure 3 shows a conventional method of updating data in the EEPROM 400 of Figure 2. In a first step E1, the data is received by the microprocessor 10 via the interface 2 and the input/output circuit 50. Each data item received is temporarily stored in the RAM 30 (step E2). In the following step E3, a zone of the EEPROM 400 containing the data to be updated is erased by means of the voltage-raising module 410 under the control of the microprocessor 10. When the register 420 indicates that erasing is complete, then the received data is extracted from the RAM 30 for writing in the above zone (step E4).

A major drawback of that method lies in the fact that it is relatively lengthy to implement. This is particularly troublesome when using contactless smart cards since it is difficult under such circumstances to control the length of time the smart card spends in the electromagnetic field of the terminal. This time depends on how fast the user handles the card. All of the operations associated with communicating with the terminal, including the operations of erasing and writing in the EEPROM, must therefore be performed as quickly as

possible. In practice, it is accepted that together these operations must not require more than a few tens of milliseconds. Unfortunately, a single transaction can require a plurality of erasing and writing operations in the memory, and each of those operations on its own can require several milliseconds.

SUMMARY OF THE INVENTION

The present invention seeks to reduce the time required for processing a write command that comprises a definition of a memory zone followed by data to be stored in that memory zone.

To this end, the processing is carried out in the following manner. In a receiving step, the data is written into a buffer memory. In an erasure step, the memory zone defined by the write command is erased while the data is written into the buffer memory. In a transfer step, the data is transferred from the buffer memory to the memory zone defined by the write command.

Thus, the receiving step and the erasure step are, at least partially, effected in parallel. Consequently, the invention reduces the time required to process the write command concerned compared with the conventional method described hereinbefore.

The memory zone of interest may be located, for example, in an electrically erasable programmable read-only memory (EEPROM). The EEPROMs presently available on the market generally require several milliseconds to be erased. During this time, all or part of the relevant data can be received and temporarily stored in the buffer memory.

These and other characteristics and advantages of the present invention will appear on reading the following detailed description given with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

- Figure 1, described above, is a block diagram showing the electrical portion of a smart card;
- Figure 2, described above, shows greater detail of an EEPROM unit contained in the Figure 1 apparatus;
- Figure 3, described above, shows a conventional algorithm for updating data in an EEPROM; and
- Figure 4 shows an algorithm of the invention for updating data in an erasable memory.

DETAILED DESCRIPTION OF THE INVENTION

Figure 4 illustrates an algorithm in accordance with the invention. The algorithm as shown in Figure 4 is stored in the microcontroller 1 of the smart card illustrated in Figure 1. More particularly, the algorithm is stored in the ROM 20 in the form of a computer program, for example, as a subprogram in the operating system of the microcontroller 1.

It is assumed that the smart card illustrated in Figure 1 is coupled to a read/write terminal. It is further assumed that the read/write terminal applies a write command followed by data to the smart card in compliance with ISO standard 7816. An ISO 7816 command typically comprises five bytes, CLA, INS, P1, P2, P3. CLA is a byte that indicates the type of card for which the command is intended. INS is a byte that indicates the type of command. In the case of a write command, P1 and P2 are two bytes that indicate a start address and P3 is a byte that indicates the size of the data that needs to be written into the smart card in terms of number of bytes.

When the smart card receives the write command, it causes an interruption that activates the microcontroller 1 illustrated in Figure 1. The microprocessor 10 receives the write command from the read/write terminal via the interface 2 (with or without contact) and via the input/output circuit 50 illustrated in Figure 1.

In a first step F1, which is illustrated in Figure 4, the microprocessor 10 decodes the write command. Accordingly, the microprocessor recognizes, as it were, that it is going to receive update data for writing in a zone ZN of the EEPROM 400 illustrated in Figure 2. As described hereinbefore, EEPROM 400 forms part of EEPROM unit 40 illustrated in Figure 1.

In the following step F2, the microprocessor 10 determines whether the zone ZN is empty. If the response to step F2 is "no", then an operation of erasing the data contained in the zone ZN is started in a step F3, by activating the voltage-raising module 410 of the EEPROM unit 40. The zone ZN is then erased (step F3') independently of the progress of the algorithm through the microprocessor 10, as represented by dashed lines in Figure 4. Thus, while erasure is taking place, the microprocessor can receive the update data from the read/write terminal in a step F4 and can store each data item in the RAM 30 (step F5).

If step F2 determines that the zone ZN contains no data, then the microprocessor 10 waits until it has received the update data prior to implementing steps F4 and F5.

Once the update data has been received and stored in the RAM 30, and if initially the zone ZN was not empty (step F2), then in a step F6, the microprocessor verifies whether erasure of the zone ZN has terminated. To do this, the microprocessor 10 interrogates the register 420 of the EEPROM unit 40. If the flag contained in this register indicates that erasure has not terminated, then the microprocessor 10 repeatedly interrogates the register 420 at regular time intervals until this flag changes state.

Once the flag indicates that erasure has terminated during a verification performed in step F6, then the zone ZN is updated by writing therein the data stored in the RAM 30 (step F7).

If it is found in step F2 that the zone ZN is empty, then step F6 is omitted, with the algorithm passing directly from the reception and storage steps F4, F5 to the write step F7, as represented by dashed line F57.

The description hereinbefore with reference to the drawings illustrates the following basic characteristics. A write command comprises a definition of a memory zone (ZN) followed by data to be stored in that memory zone. The write command is processed in the following manner. In a receiving step (F4), the data is written into a buffer memory (RAM). In an erasure step (F3), the memory zone (ZN) defined by the write command is erased while the data is written into the buffer memory (RAM). Thus, the receiving step (F4) and the erasure step (F3) are, at least partially, effected in parallel. In a transfer step (F7), the data is transferred from the buffer memory (RAM) to the memory zone (ZN) defined by the write command.

The present invention as described above and as defined in the accompanying claims is not limited to a zone ZN constituting part only of the EEPROM 400. The zone ZN could constitute the entire erasable memory.

Furthermore, the present invention can be applied to apparatuses other than smart cards, and in particular to other types of portable appliance.

CLAIMS

1/ A method of processing a write command comprising a definition of a memory zone followed by data to be stored in that memory zone, the method comprising:

- a receiving step in which the data is written into a buffer memory;
- an erasure step in which the memory zone defined by the write command is erased while the data is written into the buffer memory; and
- a transfer step in which the data is transferred from the buffer memory to the memory zone defined by the write command.

2/ An apparatus capable of processing a write command comprising a definition of a memory zone followed by data to be stored in that memory zone, the apparatus comprising a controller which in response to said write command causes the apparatus to effect the following steps:

- a receiving step in which the data is written into a buffer memory;
- an erasure step in which the memory zone defined by the write command is erased while the data is written into the buffer memory; and
- a transfer step in which the data is transferred from the buffer memory to the memory zone defined by the write command.

3/ A smart card capable of processing a write command comprising a definition of a memory zone followed by data to be stored in that memory zone, the smart card comprising a controller which in response to said write command causes the smart card to effect the following steps:

- a receiving step in which the data is written into a buffer memory;

- an erasure step in which the memory zone defined by the write command is erased while the data is written into the buffer memory; and
- a transfer step in which the data is transferred from the buffer memory to the memory zone defined by the write command.

4/ A computer program product for a smart card, the computer program product comprising a set of instructions which, when loaded into the smart card, causes the smart card to effect the following steps in response to a write command that comprises a definition of a memory zone followed by data to be stored in that memory zone
- a receiving step in which the data is written into a buffer memory;
- an erasure step in which the memory zone defined by the write command is erased while the data is written into the buffer memory; and
- a transfer step in which the data is transferred from the buffer memory to the memory zone defined by the write command.

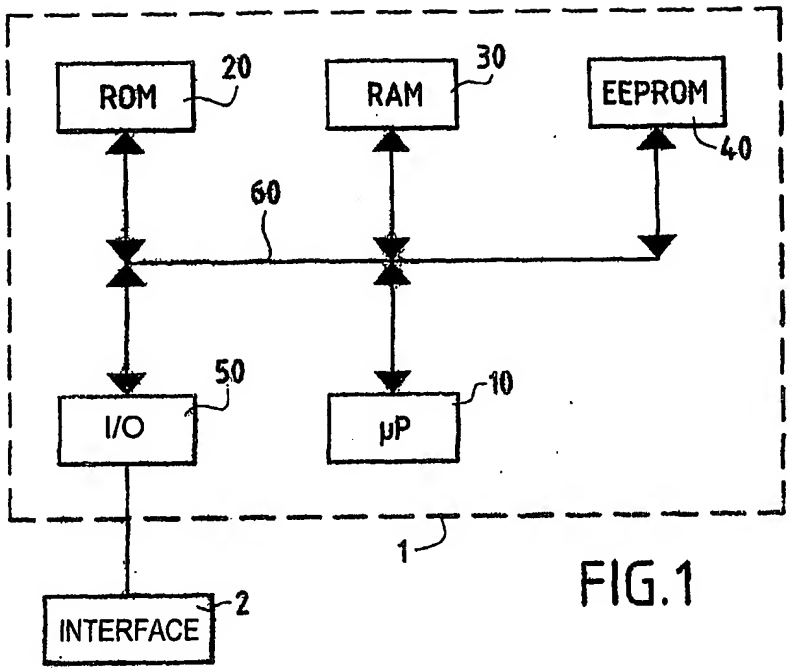

FIG.1

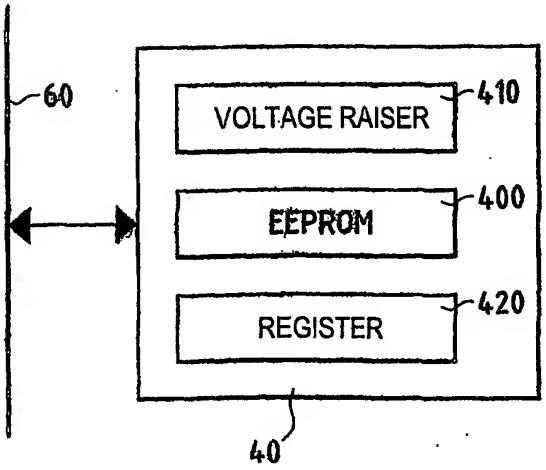

FIG.2

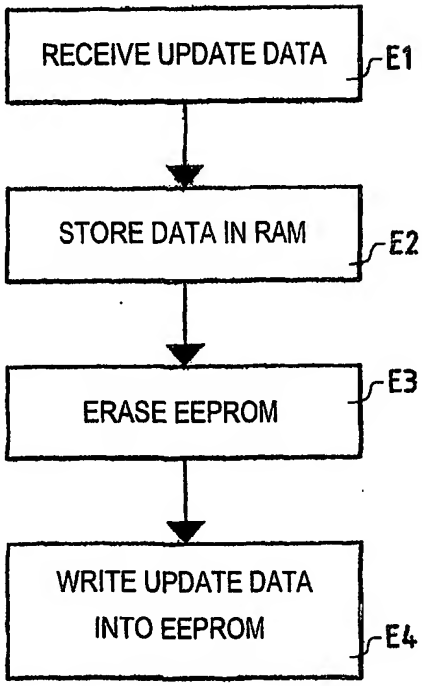

FIG.3

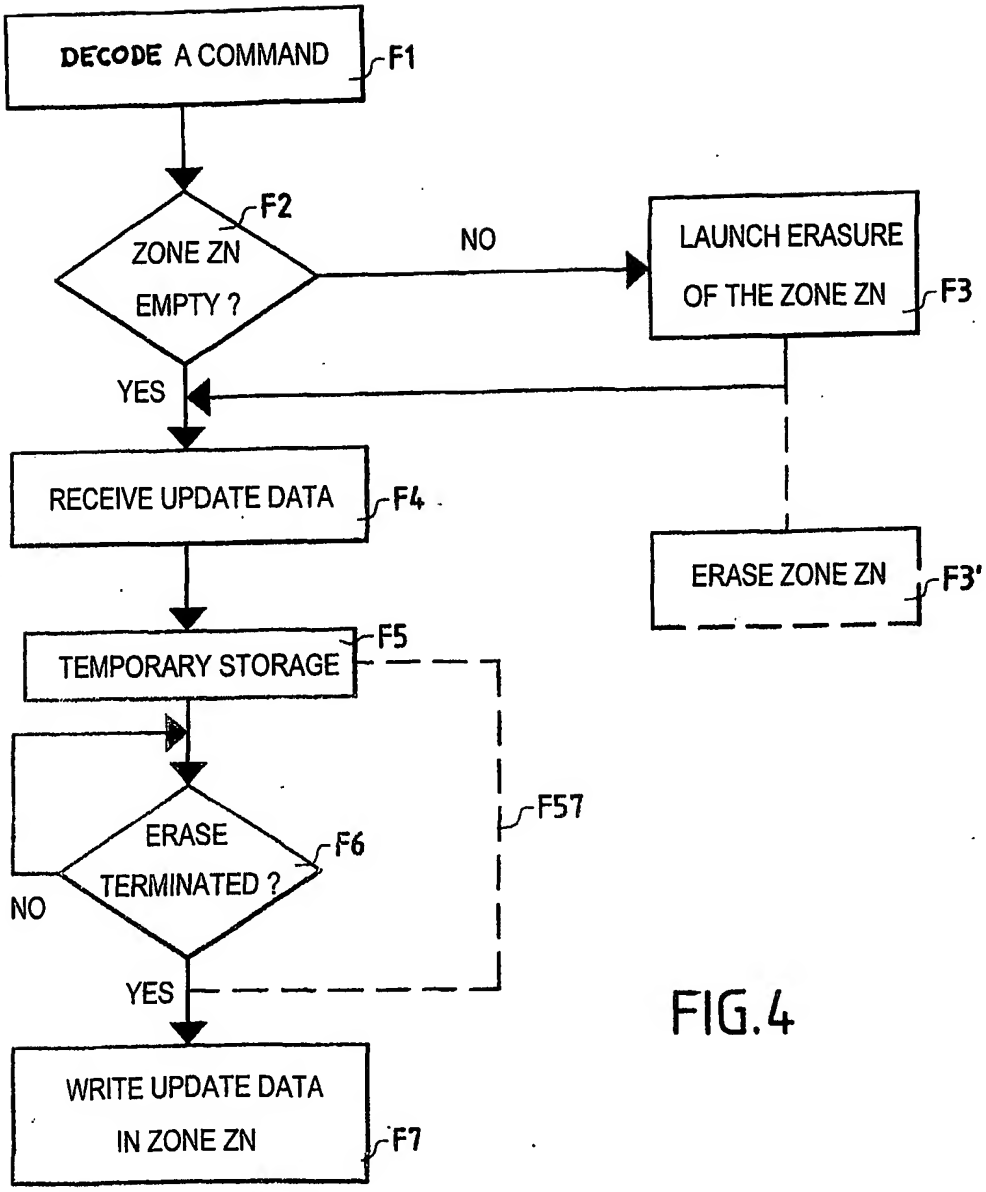
DECODE A COMMAND
F1
ZONE ZN EMPTY ?
F2
NO
LAUNCH ERASURE OF THE ZONE ZN
F3
YES
RECEIVE UPDATE DATA
F4
ERASE ZONE ZN
F3'
TEMPORARY STORAGE
F5
F57
ERASE TERMINATED ?
F6
NO
YES
WRITE UPDATE DATA IN ZONE ZN
F7

FIG.4

INTERNATIONAL SEARCH REPORT

Int onal Application No
PCT/IB 01/00862

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C16/16 G06F9/445 G11C16/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 149 (P-1708), 11 March 1994 (1994-03-11) & JP 05 324000 A (SHARP CORP), 7 December 1993 (1993-12-07) abstract	1-4
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 417 (P-1781), 4 August 1994 (1994-08-04) & JP 06 124175 A (SHARP CORP), 6 May 1994 (1994-05-06) abstract	1-4
A	EP 0 489 204 A (HEWLETT PACKARD LTD) 10 June 1992 (1992-06-10) column 2, line 12 -column 3, line 16; figure 1	1-4

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 528 280 A (TOSHIBA AVE KK ;TOKYO SHIBAURA ELECTRIC CO (JP)) 24 February 1993 (1993-02-24) column 9, line 38 -column 12, line 56; figure 3	1-4
A	US 5 761 702 A (MATSUFUJI KATSUAKI) 2 June 1998 (1998-06-02) column 2, line 1 - line 26; figure 17 column 3, line 35 -column 6, line 26; figures 1-5 column 8, line 35 -column 10, line 30; figures 9-12	1-4
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int onal Application No
PCT/IB 01/00862

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(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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Published
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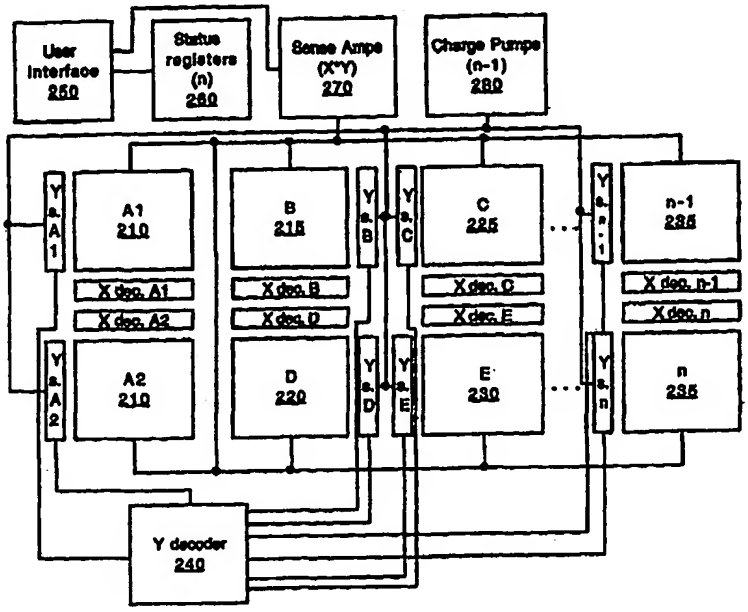
(54) Title: FLASH MEMORY PARTITIONING FOR READ-WHILE-WRITE OPERATION



(57) Abstract

A method and apparatus for partitioning a flash memory device (20) is provided. The flash memory device includes a plurality of partitions, (210, 215, 220, 225, 230), each partition able to be read, written, or erased simultaneously with the other partitions.

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FLASH MEMORY PARTITIONING FOR READ-WHILE-WRITE OPERATION

FIELD OF THE INVENTION

The present invention relates to flash memory, and more specifically, to partitioning of flash memory.

BACKGROUND

Flash memory devices are special type of EEPROM that can be erased and written to in blocks instead of one byte at a time. Some applications of the flash memory include embedded control code and data of a cellular telephone so that it can easily be updated if necessary. Flash memory may also be used in modems because it enables the modem manufacturer to support new protocols as they become standardized. Flash memory may further be used in computers to provide a basic input/output system (BIOS) that can be upgraded. Other uses are known in the art.

Figure 1 illustrates one prior art flash memory device 100. The memory 110 into which data is written has an X-decoder 160 and a Y-decoder 180 associated with it. The X-decoder 160 and Y-decoder 180 permit addressing the rows and columns of memory. A user interface 120 controls the flash memory device 100. The user interface 120 interfaces with a processor that controls access to the memory 110. A status register 130 stores the current status -- writing, reading, or erasing -- of the memory 110. The processor knows the status of the flash memory from the user interface 120.

Sense amplifiers 140 are associated with the memory 110. In one prior art implementation, the sense amplifiers are used to amplify signals for writing to and reading from the memory 110. For a row divided into sixteen input/outputs (I/Os), sixteen sense amplifiers 140 are used for writing and reading, one for each I/O. A charge pump 150 is further included in the flash memory 100. The charge pump 150 is used to provide the voltage levels needed for reading from, writing to, and erasing the memory 110. Generally, prior art flash memory devices are erased and written to as a block, consisting of a subset of memory 110. There is one set of circuitry, thus a user can not write to

one block of the flash memory while simultaneously erasing or reading another block of the memory.

Simultaneous operation is desired in some applications that are constrained by the erase time (typically 250-500 ms) of a flash memory block. For example, a cellular telephone executes code directly from the flash memory. It is advantageous to be able to erase a separate memory block to reclaim space for data storage at the same time.

One prior art solution to this problem is to have multiple flash memory devices. In that case, one device may be written to, while the other device is being erased. This has numerous disadvantages. The multiple devices take up more real-estate. Because there are multiple devices hardware is duplicated. Additionally, using multiple flash memory devices may cost more, increase power use, and decrease overall system reliability.

SUMMARY OF THE INVENTION

The present invention relates to partitioning of a flash memory device to permit read-while-write operations. The flash memory device includes a plurality of partitions, each partition able to be read, written, or erased simultaneously with the other partitions.

Other features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 illustrates a prior art flash memory device.

Figure 2 illustrates one embodiment of a multi-partitioned flash memory device.

Figure 3 illustrates one embodiment of a three partitioned flash memory device.

Figure 4 illustrates an example of a cellular telephone using a flash memory device.

DETAILED DESCRIPTION

A method and apparatus for partitioning a flash memory for read-while-write operation is described. It is an intended advantage of the present invention to permit simultaneous reading, and/or writing and/or erasing operations on a single flash memory device. It is a further intended advantage of the present invention to permit updating of code stored on a flash memory device while code is being executed.

Figure 2 illustrates a multi-partitioned flash memory device. Partitions A 210, B 215, C 225, D 220, E 230, . . . n-1 235, n 235 are illustrated. Each partition is implemented as a physically separate device on the flash memory device. For one embodiment, each partition is implemented on a different physical plane. Each of the partitions 210, 215, 220, 225, 225, 230, 235, and 240 has associated an X decoder, and a Y selector. Each of the Y selectors are coupled to a Y decoder 240, that controls the Y selectors. For an alternative embodiment, multiple Y decoders 240 may be present in the system. The X decoders and Y selectors enable selection of a specific area within flash memory 200 for access, including reading, writing, or erasing. Having multiple X selectors and Y decoders permits simultaneous access to more than one subsection of the flash memory. For example, while partition A may be erased, partition B may simultaneously be read, and partition C written to. Each of the partitions may include one or more blocks, that may be erased separately. Thus, for example, a memory in partition A may be written to, while a memory block in partition B is being erased.

A user interface 250 permits a user to control the access to the flash memory 200. For one embodiment, the user interface 250 is part of the flash memory itself. For an alternative embodiment, the user interface 250 is located on a separate chip. The interface includes a number of state machines used to control each of the write parallel operations. Thus, if there can be two parallel write operations (writing to the data block while updating the code, for example), there are two state machines. If there can be three parallel write operations, three

state machines are included. These state machines are described in more detail in the concurrently filed related application entitled ____, Serial No. ____.

Status registers are coupled to the user interface 260. The status registers 260 indicate the status of each partition. There are n partitions, and for one embodiment there are n status registers 260. The status of each partition is one of the following: idle, being read, being written to, or being erased.

Sense amplifiers 270 are coupled to the user interface 250 as well. The sense amplifiers are used in the read, write, and erase operations. For one embodiment, the number of sense amplifiers 270 is determined as follows. For a sixteen bit wide flash memory, sixteen sense amplifiers 270 are needed for each parallel executable operation. Thus, for example, if a first partition is read while a second partition is written to, 32 sense amps 270 are needed. For example, if two partitions may be read in parallel, 32 sense amps 270 are needed for reading. The number of sense amplifiers 270 is a factor of the width of the output row of the flash memory (X) times the number of parallel executable operations (Y). For one embodiment, for a three partition flash memory, for example, one partition may be read, another partition written to, and a third parting erased uses 3X sense amplifiers 270. Sense amplifiers 270 used for erasing use a very low percentage of the total erase time. Similarly, sense amplifiers 270 used for writing use a low percentage of the total write time. Therefore, for one embodiment, a single sense amp 270 is used for each parallel executable write operation and each parallel executable erase operation. The sense amp 270 is used for verifying each bit as it is written.

Additionally, redundant sense amplifiers 270 may be included for other operations, such as a redundant column access. For one embodiment, for each parallel read and/or write, two redundancy sense amplifiers 270 are included in sense amplifier block 270.

Furthermore, charge pumps 280 are included in the circuit. Charge pumps 280 are used to set the voltage level for reading, writing, and erasing. For one embodiment, the voltage level used for erasing is approximately -10 volts. For one embodiment, the voltage level used

for reading and writing is approximately 7 volts. For one embodiment, a single charge pump 280 that has multiple leads to permit parallel access to partitions is used. Alternatively, multiple separate charge pumps 280 may be used to provide the voltage levels needed for accessing the different partitions simultaneously. The charge pumps 280 are coupled to the Y-selectors of each of the partitions, to raise the voltage level to the appropriate level to read, write, or erase.

The multi-partitioned flash memory illustrated in Figure 2 may be used for a number of purposes. The number of partitions depends upon the function of the flash memory. For example, a three partitioned flash memory device is illustrated in Figure 3.

One example of using a three partitioned flash memory device is as follows. A first partition may be used to store data. A second partition may be used to store code, that is executed by an apparatus that includes the flash memory device. The third partition may be used to permit updating of the code. Thus, for example, if the code changes as a result of an update, new code is written to the third partition while the original code in the second partition is concurrently executing. When the new code has been written and verified, the third partition can become the partition used for the code. Thus, seamless updating of flash memory devices is possible. Another example of a three partitioned flash memory device is having code executed from a first partition, while updating data in a second partition. Thus, for example, if the code execution results in an updating of data, this can be accomplished seamlessly.

Figure 3 illustrates one embodiment of a three partitioned flash memory device. Partition A 310, partition B 315, and partition C 320 each have an associated X decoder and Y select, and can be accessed separately. The layout illustrated in Figure 3 corresponds to one embodiment of an actual layout of a flash memory device. The X decoder 307 and Y select 309 and 312 are associated with Partition A 305, 310. For one embodiment, partition A 310 is split in half by Y selectors 309, 312. The splitting of partition A 310 is for layout purposes, such that a first part of partition A 310 is aligned with partition B, while the other part of partition A 305 is aligned with

partition C. For one embodiment, the splitting of partition A 310 optimizes performance for read speed. The Y selectors 309 and 312 are coupled to Y decoder 325. Additionally, a status register 335 is associated with partition A. The status register 335 indicates the status of partition A -- idle, being written to, being read from, or being erased. Similarly, for partition B, there is an X decoder 317, Y select 319, and a status register 340. Partition C also includes an X decoder 323, a Y select 322, and a status register 345. For one embodiment, a single user interface 330 is coupled to the status registers 335, 340, 345 for each of the partitions.

Sense amplifiers 350 support all of the partitions. For one embodiment, the number of sense amplifiers is eighteen. Sixteen sense amplifiers 350 are used for a read operation to one of the partitions. One sense amplifier is used for a parallel write operation from one of the partitions. The interface includes a number of state machines used to control each of the parallel write operations. Thus, if there can be two parallel write operations (writing to two partitions simultaneously), there are two state machines.

The number of charge pumps 360 also parallels the number of parallel operations. For another embodiment, the number of connections to a single charge pump 360 equals the number of parallel operations. Each of these connections may be held at a different voltage level, permitting multiple operations using different voltage levels. For one embodiment, a separate connection is coupled to the decoders associated with each partition. Thus, a first connection is coupled to a first partition, a second connection is coupled to a second partition, and so on. Thus, each connection outputs a variety of voltage levels, corresponding to each of the operations that may be executed on the partition. For another embodiment, a first connection outputs a first voltage level for writing, a second connection outputs a second voltage level for reading, and a third connection outputs a third voltage level for erasing. In this instance, switches couple the appropriate partition to the appropriate connection for the operation about to be performed.

Figure 4 illustrates an example of a cellular telephone using a flash memory device. The cellular telephone 410 includes a flash

memory device 430. Although the flash memory device 430 is illustrated on the cellular phone 410, it is understood that generally the flash memory device 430 is received in a receptacle within the body of the cellular telephone 410.

The cellular phone 410 illustrated is active. That is, it is executing code. The partition 460 that includes the currently active code is being executed. The use of such code is known in the art. Another partition 450 includes dialing or voice data. For example, the cell phone 410 may include a dialing director, or similar data in the data partition 450. A third partition 470 is receiving new code 440 from outside. For one embodiment, the third partition may be updated remotely. Thus, while the cellular telephone is active, the code in the code partition 460 may be executed, while simultaneously new code 440 is written to the new code partition 470, and the data partition 450 is used to recall dialing data. In this way, the cellular telephone permits seamless updating of its code, and concurrent updating and use of the cellular telephone. Other applications of such seamless code updating may be similarly implemented.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense. The present invention should not be construed as limited by such embodiments and examples, but rather construed according to the following claims.

CLAIMS

What is claimed is:

1. A flash memory device comprising:

a plurality of partitions of the flash memory device, each partition able to be written, read, or erased simultaneously with the other partitions.

2. The flash memory device of claim 1, further comprising:

an plurality of x decoders, each x decoder associated with a partition; and

a plurality of y decoders, each y decoder associated with a partition.

3. The flash memory device of claim 1, further comprising a plurality of sense amplifiers.

4. The flash memory device of claim 3, wherein the plurality of sense amplifiers comprising:

a first plurality of sense amplifiers for each simultaneously executable read operation; and

at least one sense amplifier for each simultaneously executable erase and write operation.

5. The flash memory device of claim 4, wherein the first plurality of sense amplifier comprises a plurality of sense amplifiers for each parallel read operation.

6. The flash memory device of claim 1, further comprising a charge pump for providing a voltage output.

7. The flash memory device of claim 6, wherein the charge pump provides a plurality of voltage outputs.

8. The flash memory device of claim 7, wherein the plurality of voltage outputs corresponds in number to the plurality of

partitions of the flash memory device, thereby providing a voltage output for each partition.

9. The flash memory device of claim 1, further comprising a plurality of status registers.

10. The flash memory device of claim 9, wherein the plurality of status registers corresponds to the plurality of partitions of the flash memory device.

11. A system comprising:

a bus;

a processor coupled to the bus; and

a memory coupled to the bus and accessible by the processor, the memory including a flash memory, the flash memory comprising a plurality of partitions, each of the partitions separately readable, writable, and erasable.

12. The flash memory device of claim 11, further comprising:

an plurality of x decoders, each of the x decoders associated with a partition;

a plurality of y decoders, each of the y decoders associated with a partition.

13. The flash memory device of claim 11, further comprising a plurality of sense amplifiers.

14. The flash memory device of claim 13, wherein the plurality of sense amplifiers comprising:

a first plurality of sense amplifiers for each simultaneously executable read operation; and

at least one sense amplifier for each simultaneously executable erase and write operation.

15. The flash memory device of claim 14, wherein the first plurality of sense amplifier comprises sixteen sense amplifiers for each parallel read operation.

16. The flash memory device of claim 11, further comprising a charge pump for providing a voltage output.

17. The flash memory device of claim 16, wherein the charge pump provides a plurality of voltage outputs.

18. The flash memory device of claim 17, wherein the plurality of voltage outputs corresponds in number to the plurality of partitions of the flash memory device, thereby providing a voltage output for each partition.

19. The flash memory device of claim 11, further comprising a plurality of status registers.

20. The flash memory device of claim 19, wherein the plurality of status registers corresponds to the plurality of partitions of the flash memory device.

21. A method of simultaneously accessing and erasing a flash memory, the flash memory including a first partition, a second partition, and a third partition, the method comprising:

accessing the first partition or the second partition; and

simultaneously erasing the third partition.

22. The method of claim 21, wherein said step of accessing comprises reading from or writing to the first partition or the second partition.

23. The method of claim 21, wherein said step of erasing comprises the step of:

applying a first voltage level to the third partition.

24. The method of claim 23, wherein said step of accessing comprises the step of:

applying a second voltage level to the first or the second partition.

25. The method of claim 24, wherein said second voltage level is lower than said first voltage level.

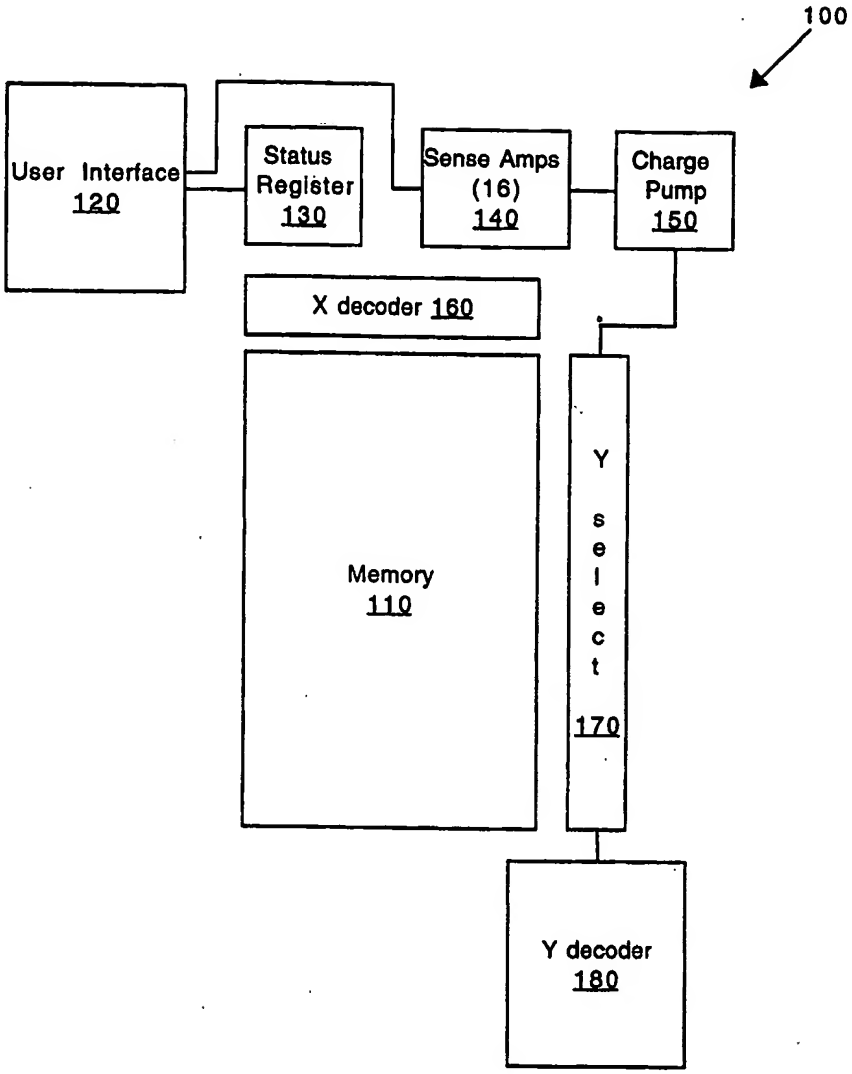

Fig. 1 (Prior Art)

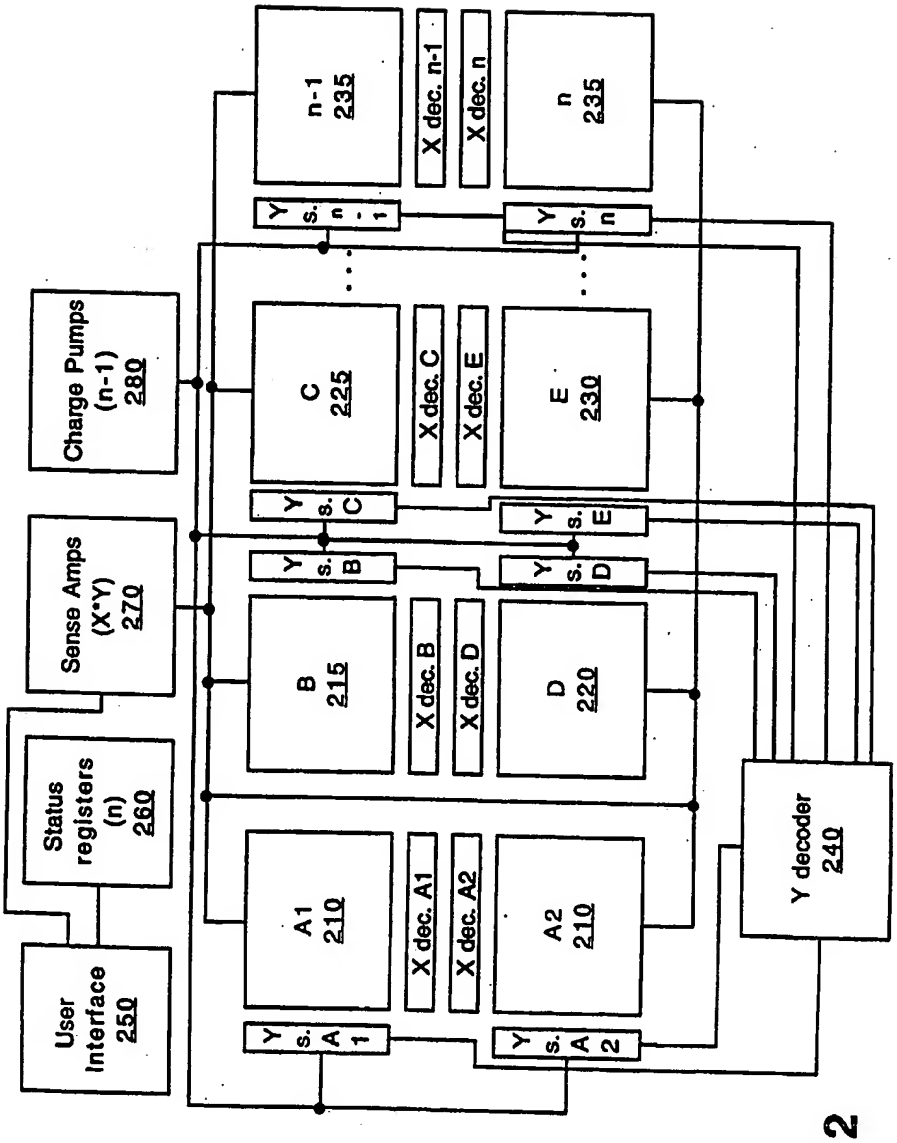
n-1
235
X dec. n-1
X dec. n
n
235
Y s. n-1
Y s. n
Charge Pumps
(n-1)
280
C
225
X dec. C
X dec. E
E
230
Y s. C
Y s. E
Sense Amps
(X*Y)
270
Y s. B
Y s. D
B
215
X dec. B
X dec. D
D
220
Status
registers
(n)
260
A1
210
X dec. A1
X dec. A2
A2
210
Y decoder
240
User
Interface
250
Y s. A1
Y s. A2

Fig. 2

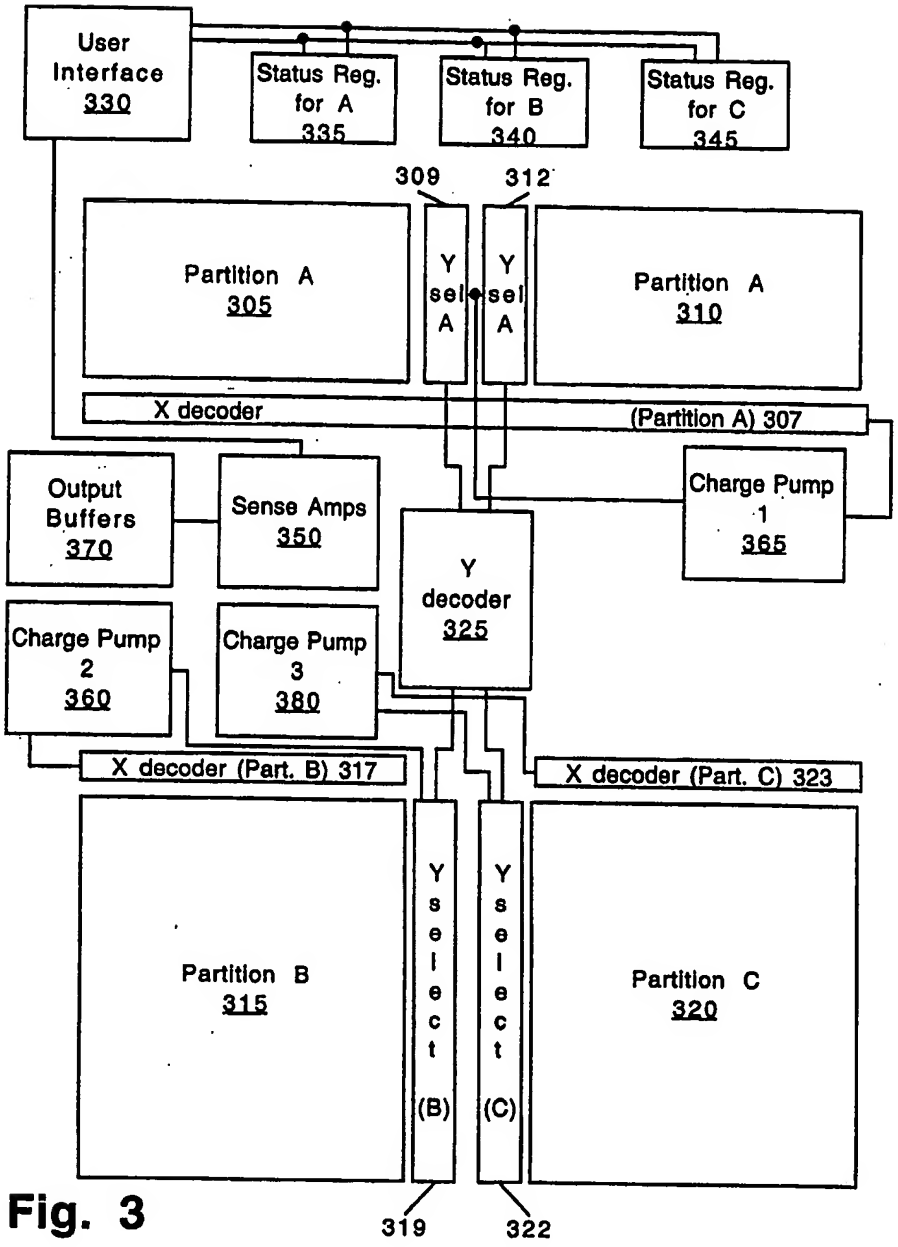
User Interface 330
Status Reg. for A 335
Status Reg. for B 340
Status Reg. for C 345
309
312
Partition A 305
Y sel A
Y sel A
Partition A 310
X decoder (Partition A) 307
Output Buffers 370
Sense Amps 350
Charge Pump 1 365
Y decoder 325
Charge Pump 2 360
Charge Pump 3 380
X decoder (Part. B) 317
X decoder (Part. C) 323
Partition B 315
Y select (B)
Y select (C)
Partition C 320
319
322

Fig. 3

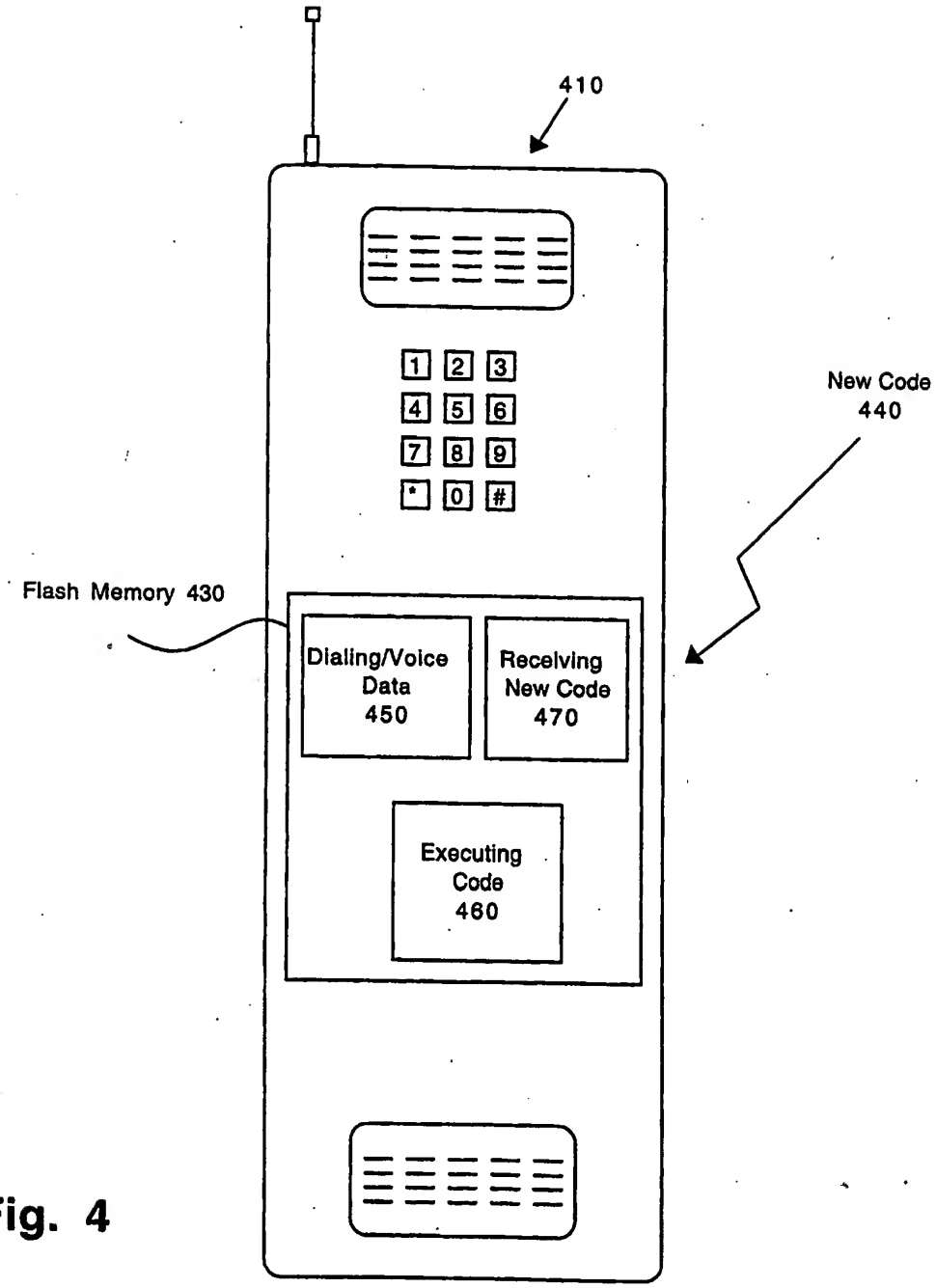
410
New Code
440
1 2 3
4 5 6
7 8 9
* 0 #
Flash Memory 430
Dialing/Voice Data 450
Receiving New Code 470
Executing Code 460

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/25217

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :G11C 16/04
US CL :365/185.11,185.33,185.29,189.04
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 365/185.11,185.33,185.29,189.04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
U.S. PTO APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 5,748,528 A (CAMPARDO et al.) 05 May 1998 (05/05/98) see entire document.	1-25

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"B"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 05 MARCH 1999	Date of mailing of the international search report 15 APR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer D. NELMS Telephone No. (703) 308-0089

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